[0024] What is claimed is:

1. A method for indexing a plurality of ordered elements stored in bit-reversed order in a first and a second memory space, wherein said first memory space is indexed by a first memory index denoting the memory positions in said first memory space, wherein said second memory space is indexed by a second memory index denoting the memory positions in said second memory space, and wherein the logical position of each of said elements within said plurality of ordered elements is indexed by an element index, the method comprising:

   bit-reversing the element index of a selected one of said elements;

   locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed element index equals 0 and said second memory space where the MSB of said bit-reversed element index equals 1; and

   locating the position of said selected element within said MSB-located memory space at the memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed element index.

2. A method according to claim 1 wherein said indices are binary indices, wherein there are n of said elements, wherein said memory indices each comprise s digits where $n/2$ equals 2^s, and wherein said element index comprises t digits where n equals 2^t.

3. A method for indexing n ordered elements stored in bit-reversed order in a first and a second memory space, wherein said first memory space is indexed by a first binary memory index denoting the memory positions in said first memory space, wherein said second memory space is indexed by a second binary memory index denoting the memory positions in said second memory space, and wherein the logical position of each of said elements within said plurality of ordered elements is indexed by a binary element index, the method comprising:

   bit-reversing the binary element index of a selected one of said elements;

   locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed binary element index equals 0 and said second memory space where the MSB of said bit-reversed binary element index equals 1; and

locating the position of said selected element within said MSB-located memory space at the memory binary index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed binary element index,

wherein said binary memory indices each comprise s digits where $n/2$ equals 2^s, and wherein said binary element index comprises t digits where n equals 2^t.

4. A Digital Signal Processing architecture capable of storing a plurality of ordered elements in bit-reversed order in a first and a second memory space, the architecture comprising:

a first memory index denoting the memory positions in said first memory space;

a second memory index denoting the memory positions in said second memory space;

an element index denoting the logical position of each of said elements within said plurality of ordered elements;

means for bit-reversing the element index of a selected one of said elements;

means for locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed element index equals 0 and said second memory space where the MSB of said bit-reversed element index equals 1; and

means for locating the position of said selected element within said MSB-located memory space at the memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed element index.

5. An architecture according to claim 4 wherein said indices are binary indices, wherein there are n of said elements, wherein said memory indices each comprise s digits where $n/2$ equals 2^s, and wherein said element index comprises t digits where n equals 2^t.

6. An architecture according to claim 4 and further comprising means for creating any of said indices.

7. A Digital Signal Processing architecture capable of storing n ordered elements in bit-reversed order in a first and a second memory space, the architecture comprising:

a first binary memory index denoting the memory positions in said first memory space;

a second binary memory index denoting the memory positions in said second memory space;

a binary element index denoting the logical position of each of said elements within said n ordered elements;

means for bit-reversing the binary element index of a selected one of said elements;

means for locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed binary element index equals 0 and said second memory space where the MSB of said bit-reversed binary element index equals 1; and

means for locating the position of said selected element within said MSB-located memory space at the binary memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed binary element index,

wherein said binary memory indices each comprise s digits where $n/2$ equals 2^s, and wherein said binary element index comprises t digits where n equals 2^t.

8. A Digital Signal Processor comprising:

a first memory space and a second memory space collectively capable of storing a plurality of ordered elements in bit-reversed order;

first memory indexing means operative to denote in a first memory index the memory positions in said first memory space;

second memory indexing means operative to denote in a second memory index the memory positions in said second memory space;

element indexing means operative to denote in an element index the logical position of each of said elements within said plurality of ordered elements; and

processing means comprising:

means for bit-reversing the element index of a selected one of said elements;

means for locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed element index equals 0 and said second memory space where the MSB of said bit-reversed element index equals 1; and

means for locating the position of said selected element within said MSB-located memory space at the memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed element index.

9. A processor according to claim 8 wherein said indices are binary indices, wherein there are n of said elements, wherein said memory indices each comprise s digits where $n/2$ equals 2^s, and wherein said element index comprises t digits where n equals 2^t.

10. A Digital Signal Processor comprising:

a first memory space and a second memory space collectively capable of storing n ordered elements in bit-reversed order;

first memory indexing means operative to denote in a first binary memory index the memory positions in said first memory space;

second memory indexing means operative to denote in a second binary memory index the memory positions in said second memory space;

element indexing means operative to denote in a binary element index the logical position of each of said elements within said n ordered elements; and

processing means comprising:

means for bit-reversing the binary element index of a selected one of said elements;

means for locating said selected element as being in either of said first memory space where the most significant bit (MSB) of said bit-reversed binary element index equals 0 and said second memory space where the MSB of said bit-reversed binary element index equals 1; and

means for locating the position of said selected element within said MSB-located memory space at the binary memory index of said MSB-located memory space that corresponds to the non-MSB bits of said bit-reversed binary element index,

wherein said binary memory indices each comprise s digits where $n/2$ equals 2^s, and wherein said binary element index comprises t digits where n equals 2^t.